In the Claims:

Please amend claims 1-3, 7-8, 10, 12-16, and 21. The claims are as follows:

1. (Currently Amended) An integrated circuit, comprising:

a pulse generator ~~adapted to generate~~ for generating a pulsed signal;

a cycle counter ~~adapted to count~~ for counting cycles of said pulsed signal;

one or more repairable circuit elements; and

a repair processor ~~adapted to repair~~ for repairing a repairable circuit element of said one or more circuit elements when said cycle counter reaches a pre-determined cycle count.

2. (Currently Amended) The integrated circuit of claim 1, wherein said repair processor[[,]] ~~replaces~~ is adapted to permanently disable said repairable element and replace said repairable circuit element with a redundant circuit element having the same function as said repairable circuit element.

3. (Currently Amended) The integrated circuit [[if]] of claim 1, wherein said pulsed signal is a clock signal and said repairable circuit element is responsive to said clock signal.

4. (Currently Amended) The integrated circuit of claim 1, further including a memory circuit ~~adapted to store~~ for storing a cycle count of the number of cycles counted since an initial power up and to resume counting from said stored cycle count after a power down/power up cycle of said integrated circuit.

5. (Original) The integrated circuit of claim 1, wherein:

said cycle counter is adapted to generate a trigger signal when said predetermined cycle count is reached; and

said repair processor is adapted to receive said trigger signal and affect a repair of said repairable circuit element when said trigger signal is received.

6. (Original) The integrated circuit of claim 5, wherein said trigger signal comprises a subset of a set of bits encoding a current cycle count of said cycle counter.

7. (Currently Amended) The integrated circuit of claim 1, wherein said repairable circuit element is selected from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic gate, a group of logic gates, an individual device[[s]], a transistor, a diode, a resistor[[s]], capacitor, an inductor and a wire.

8. (Currently Amended) The integrated circuit of claim 1, wherein said repairable circuit element is implemented in a field programmable gate array and said repair processor ~~programs~~ is adapted to program a replacement of selected gates of said field programmable gate array with previously unused gates of said field programmable gate array.

9. (Original) The integrated circuit of claim 1, further including a fuse bank for storing information used to implement a repair of said repairable circuit element.

10. (Currently Amended) The integrated circuit of claim 1, wherein [[in]] said repair processor is adapted to perform multiple repairs by repairing previously repaired repairable circuit elements.

11. (Original) The integrated circuit of claim 1, further including:

a redundant cycle counter; and

wherein said repair processor is adapted to replace said cycle counter with said redundant cycle counter when said cycle counter reaches a fixed cycle count.

12. (Currently Amended) A method of preemptively repairing an integrated circuit, comprising:

(a) providing a pulse generated adapted to generate a pulsed signal;

(b) providing a cycle counter adapted to count cycles of said pulsed signal;

(c) providing one or more repairable circuit elements; ~~and~~

(d) providing a repair processor adapted to repair a repairable circuit element of said one or more repairable circuit elements when said cycle counter reaches a pre-determined cycle count; and

(e) repairing said repairable circuit element when said cycle counter reaches said pre-determined cycle count.

13. (Currently Amended) The method of claim 12, wherein said step [[(d)]] (e) includes permanently disabling said repairable element and replacing said ~~one or more~~ repairable circuit element with a redundant circuit element having the same function as said repairable circuit element.

14. (Currently Amended) The method [[if]] of claim 12, wherein said pulsed signal is a clock signal and said repairable circuit element is responsive to said clock signal.

15. (Currently Amended) The method of claim 12, further including a memory circuit ~~adapted to store~~ for storing a cycle count of a number of cycles counted since an initial power up and to resume counting from said stored cycle count after a power down/power up cycle of said integrated circuit.

16. (Currently Amended) The method of claim 12, ~~wherein~~ further including:

said cycle counter ~~is adapted to generate~~ generating a trigger signal when said predetermined cycle count is reached; and

said repair processor is ~~adapted to receive~~ receiving said trigger signal and ~~affect a repair of~~ repairing said repairable circuit element when said trigger signal is received.

17. (Original) The method of claim 16, wherein said trigger signal comprises a subset of a set of bits encoding a current cycle count of said cycle counter.

18. (Original) The method of claim 12, wherein said repairable circuit element is selected from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic gate, a group of logic gates, an individual device, a transistor, a diode, a resistor, a capacitor, an inductor and a wire.

19. (Original) The method of claim 12, wherein said repairable circuit element is implemented in a field programmable gate array and said repair processor programs a replacement of selected gates of said field programmable gate array with previously unused gates of said field programmable gate array.

20. (Original) The method of claim 12, further including providing a fuse bank for storing information used to implement a repair of said repairable circuit element.

21. (Currently Amended) The method of claim 12, further including ~~wherein in~~ said repair processor ~~is adapted to perform~~ performing multiple repairs by repairing previously repaired repairable circuit elements.

22. (Original) The method of claim 12, further including:

providing a redundant cycle counter; and

said repair processor automatically replacing said cycle counter with said redundant cycle counter when said cycle counter reaches a fixed cycle count.

23. (Withdrawn) A method for designing a repairable integrated circuit, comprising:

generating an integrated circuit design from a design library of circuit elements;

simulating said integrated circuit design and generating a switching report for circuit elements of said integrated circuit design;

selecting a circuit element responsive to a pulsed signal of said integrated circuit design based on said switching report;

selecting a repairable circuit element from said design library, said repairable circuit element having the same function as said selected circuit element and allowing multiple connection paths; and

inserting said selected repairable circuit element, a cycle counter adapted to count cycles of said pulsed signal and repair processor adapted to repair said repairable circuit element when said cycle counter reaches a pre-determined value into said integrated circuit design.

24. (Withdrawn) The method of claim 23, wherein said switching report indicates a number of state toggles of each selected circuit element performed during said simulation.

25. (Withdrawn) The method of claim 23, wherein said repairable circuit element is selected from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic gate, a group of logic gates, an individual device, a transistors, a diode, a resistor, a capacitor, an inductors and a wire.

26. (Withdrawn) The method of claim 23, wherein said repairable circuit element is implemented in a field programmable gate array having spare gates and said repair processor includes a circuit for programming said field programmable array to use programmed spare gates in place of the gates originally programmed to implement said repairable circuit element.

27. (Withdrawn) A computer system comprising a processor, an address/data bus coupled to said processor, and a computer-readable memory unit adapted to be coupled to said processor, said memory unit containing instructions that when executed by said processor implement a method

for a method for designing a repairable integrated circuit, said method comprising the computer implemented steps of:

generating an integrated circuit design from a design library of circuit elements;

simulating said integrated circuit design and generating a switching report for circuit elements of said integrated circuit design;

selecting a circuit element responsive to a pulsed signal of said integrated circuit design based on said switching report;

selecting a repairable circuit element from said design library, said repairable circuit element having the same function as said selected circuit element and allowing multiple connection paths; and

inserting said selected repairable circuit element, a cycle counter adapted to count cycles of said pulsed signal and repair processor adapted to repair said repairable circuit element when said cycle counter reaches a pre-determined value into said integrated circuit design.

28. (Withdrawn) The system of claim 27, wherein said switching report indicates a number of state toggles of said circuit element performed during said simulation.

29. (Withdrawn) The system of claim 27, wherein said repairable circuit element is selected from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic gate, a group of logic gates, an individual device, a transistor, a diode, a resistor, a capacitor, an inductor and a wire.

30. (Withdrawn) The method of claim 27, wherein said repairable circuit element is implemented in a field programmable gate array having spare gates and said repair processor includes a circuit for programming said field programmable array to use programmed spare gates in place of the gates originally programmed to implement said repairable circuit element.